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RELIABILITY EVALUATION OF COMPUTER SYSTEMS.(U)
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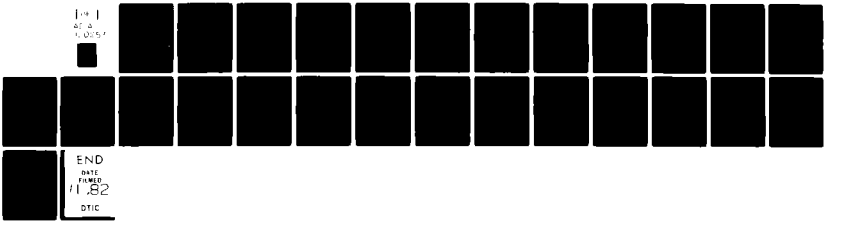

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Center for Reliable Computing

RELIABILITY EVALUATION OF COMPUTER SYSTEMS

FINAL SCIENTIFIC REPORT

AIR FORCE OFFICE OF SCIENTIFIC RESEARCH

Contract No. F49620-79-C-0069

May 1, 1979 to October 31, 1980

Principal Investigator: Prof. Edward J. McCluskey

Submitted by

CENTER FOR RELIABLE COMPUTING
COMPUTER SYSTEMS LABORATORY
Departments of Electrical Engineering and Computer Science
Stanford University
Stanford, California 94305

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ABSTRACT

This report summarizes the research conducted at the Center for Reliable Computing with the approval of the Air Force Office of Scientific Research under Contract No. F49620-79-C-0069 for the period, 1 May 1979 to 31 October 1980. Major results and current work, in various aspects of computer system reliability evaluation and design, are described.

Table of Contents

1 INTRODUCTION

This scientific report describes the research activities at the Center for Reliable Computing (CRC), Stanford University Computer Systems Laboratory, during the period May 1, 1979 to October 31, 1980.

The principal research results described are:

1. Statistical study of system utilization and failures at Stanford Linear Accelerator Center (SLAC) Computer Facility.

2. A statistical approach towards modeling uncertainty in system reliability due to uncertainty in failure rate estimation.

3. Consistency checking for generating reliable designs.

4. Testability considerations in digital system design.

In section 2 we summarize the important results in each of the above problem areas.

2 RESEARCH DESCRIPTION

2.1 Computer Reliability and Effect on Utilization

A broad-based survey of techniques for building reliable computing systems was presented in [McCluskey, 1980]. Various methods for providing specific types of fault tolerance were discussed. The types of malfunctions in a computer system and the possible responses to these malfunctions were described. A critical review of techniques for obtaining these responses was also made.

[Miller, 1979] presented a taxonomy of fault-tolerant

techniques. The paper placed the many classes of fault-tolerant techniques in a hierarchy ordered by technical characteristics. Such an approach provides a basis for presenting and comparing the techniques in a logical manner.

Major effort was concentrated on the study of failures and system load. Two large computer complexes at Stanford University have reliability data available for study. Fortunately, SLAC (the Stanford Linear Accelerator Center) and CIT (the Center for Information Technology) are functionally similar and are composed of similar equipment. This makes direct comparison of study results possible. The physical system organizations, both component interconnection and component redundancy, are quite different. The workload and levels of utilization vary considerably between the two installations.

The availability of both human-collected and machine-recorded failure data, along with corresponding load/performance data provides a unique opportunity to study the effect of utilization levels on component and system failures.

Initial work was built upon prior research at CRC [Beaudry, 1979] which was concerned with the relationships between time-of-day and various types of failures at the SLAC triplex. The time-of-day aspect of failure modeling aroused interest in the overall profile of system load.

Prior to an investigation of load, an independent analysis of the failure data was performed. Gross measures of MTBF, MTTR, and

system availability were computed for important categories of failure. In particular, hardware, software, operator-induced, and utility/facility failures were separately analyzed both for component-only and system outages. The results were reported in [Butner, 1980a].

A preliminary search for available load/performance data indicated an enormous quantity of SMF (IBM System Management Facility) raw data. An entire high-density 2400-foot magnetic tape contains approximately 24 days of these highly detailed SMF records. By contrast, the total SLAC failures amount to only 5-6 per day (1500-2000 per year). Thus, an early challenge was to meaningfully reduce the voluminous performance data in order to allow direct manipulation and comparison with a year of failure data.

The performance data is collected automatically by the IBM system software. There are approximately 50 different types of SMF data. The data contain information on the initiation, processing, and termination of jobs, on batch streams, on interactive user sessions, and on other important events. Initially, the "job step" record was selected for processing. This record corresponds one-to-one to an executed batch user job step. The record includes CPU time, step-elapsed time, I/O counts by device, paging, and other performance and accounting data. From this record four data elements were chosen for study:

- o PAGING --- the sum of page-ins and page-outs for the step.
- o EXCPS --- the sum of all I/O initiations for the step.
- o CPU --- the central processor time used for the step.

o HOUR --- the hour of the day during which the job started.

Job steps which were never executed and those corresponding to continuously-running system jobs (e.g. WYLBUR) were discarded.

From the reduced data, four "virtual day" load profiles were formed. The four load measures were job steps executed per hour, paging rate per hour, user CPU time per hour, and I/O starts per hour. The virtual day profiles depicted the average value of each load measure for each hour of the day. The profiles were statistically compared with average failure rates by hour. Final results of regression and analysis of variance were presented at FTCS-10 [Butner, 1980b].

Other reliability work was devoted to a very important (though much neglected) practical problem in reliability prediction. This is the study of the effect of uncertainty in failure rate estimation on system reliability. The problem is particularly acute in ultra-reliable systems where, failures are low and hence, the uncertainty in estimation is high. Two approaches to modeling this phenomenon were developed: the first exact and the second approximate. The usefulness of such models was illustrated using real, manufacturer provided, data on system failures. The results were presented at FTCS-10 [Iyer, 1980].

2.2 Consistency Checking

A crucial requirement in the design of high reliability multi-

processor systems, was the maintenance of consistency among processing units. In particular, consistency concerning their concept of time (affecting synchronization), their output (affecting reliable performance), and their concept of the integrity of the whole system (affecting reliable reconfiguration).

Some recent systems have chosen to solve the consistency problem in software algorithms, (as in Pluribus and SIFT), in order to allow themselves more flexibility and lower hardware costs. However, several advantages are offered by hardware implementations, such as efficiency and greater testability.

The design of the Consistency Unit (CU) [Fu, 1980a] was a demonstration of the concept of implementing a fault-tolerant algorithm in hardware using Very Large-Scale Integrated (VLSI) circuit techniques. This unit acts as an intelligent inter-processor bus interface in a four-processor system in such a way that any failure in a single processor and its associated bus cannot affect the consistency of the data exchanged among the remaining processors.

The actual design of the integrated circuit was carried out, implementing a CU for 4-bit words in an NMOS chip of about 100 mil square. This integrated circuit is also fully testable, due mainly to the structure of its design. The contents of all of its registers can be observed and the combinational part of the circuit is also directly testable.

An extended design of the CU is the Communication Interface

(CI) [Fu, 1980b]. The communication structure is regarded as being most critical in a fault-tolerant, multi-computer computer environment. The CI takes into account some practical problems in ultra-reliable systems. Specifically, the aspects of fault detection and concurrently testable hardware are addressed. In addition, the CI reports a Consistent Communication Matrix (CCM) of values for its associated processor to evaluate the integrity of the communication system as a whole.

The concept of implementing these fault-tolerant algorithms in hardware is not restricted by the designs of particular circuits. Applications could be made in new computer architectures; one candidate is the data-flow multiprocessor, which shares some architectural similarities with the CI.

Thus, the CI provides the means to generate a fault-tolerant multiprocessor system in which consistency among processors for critical functions are guaranteed. The merit of consistency is the independence of any assumptions on the possible faults that may occur, as long as they exist in a limited number of processor modules.

2.3 Testability Considerations in Design

With the advent of VLSI technology, testability considerations are assuming an ever increasing role in circuit design. [McCluskey, 1979b] presented a survey of techniques for testing of digital systems as well as methods for the design of easily testable systems; an

extensive bibliography was also included. In addition [Hayes, 1979; 1980], discussed testability considerations in microprocessor-based design. General issues relating to testability, testing methods and fault modeling were presented. In addition, specific techniques for testable design of micro-processor based systems were also discussed.

A new technique for designing easily testable sequential machines with an arbitrary number of inputs was proposed in [Pradhan, 1980]. The design was shown to be optimal with respect to the length of transfer and distinguishing sequences. An efficient checking sequence for fault detection for the proposed design was also presented.

3 REFERENCES

[Beaudry, 1980] Beaudry, M.D., "Stochastic Behavior of Failures in Computing Systems," Tech. Note No. 172, Computer Systems Laboratory, Stanford University, Stanford, California, February 1980.

[Beaudry, 1979] Beaudry, M.D., "A Statistical Analysis of failures in the SLAC Computing Center," Digest of Papers, Spring COMPCON 79, pp. 49-52, San Francisco, California, February 26 - March 1, 1979.

[Butner, 1980a] Butner, S.E. and R.K. Iyer, "A Statistical Study of Reliability and System Load at SLAC," Tech. Rpt. No. 188, Computer Systems Laboratory, Stanford University, Stanford, California, January 1980.

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[CRC, 1980] Center for Reliable Computing, "10th Annual International Symposium on Falt-Tolerant Computing Preprints," Tech. Note No. 177, Computer Systems Laboratory, Stanford University, Stanford, California, June 1980.

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[Fu, 1980b] Fu, P.L., "A Communication Interface for Fault-Tolerant Multi-Computers," paper submitted to the 11th Int. Sym. on Fault-Tolerant Computing.

[Hayes, 1979] Hayes, J.P., and E.J. McCluskey, "Testability Considerations in Microprocessor-Based Design," Tech. Report No. 179, Computer Systems Laboratory, Stanford University, Stanford California, November 1979.

[Hayes, 1980] Hayes, J.P. and E.J. McCluskey, "Testability Considerations in Microprocessor-Based Design,Computer, pp. 17-26 March 1980; reprinted in Tutorial: Microcomputer System Software and Languages, Belton E. Allen, editor, IEEE Catalog No. EHO 174-3 Library of Congress No. 80-84352, 1980.

[Iyer, 1980] Iyer, R.K., "A Study of the Effect of Uncertainty in Failure Rate Prediction on System Reliability," 10th Annual Symposium on Fault-Tolerant Computing (FTCS-10), pp. 219-224, Kyoto, Japan, October 1-3, 1980.

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[Khodadad, 1979] Khodadad-M, B., "Parity Prediction in Combinational Circuits," Proc., Ninth Annual Symposium on Fault-Tolerant Computing (FTCS-9, pp. 185-188, Madison, Wisconsin, June 20-22, 1979.

[McCluskey, 1980a] McCluskey, E.J., "Reliable Computing Systems," Tech. Note No. 182, Computer Systems Laboraory, Stanford University, Stanford, California, October 1980.

[McCluskey, 1980b] McCluskey, E.J., "Reliable Computing Systems," Technical Note No. 182, Computer Systems Laboratory, Stanford University, Stanford, California, October 1980.

[McCluskey, 1979a] McCluskey, E.J., "Designing with PLA's," Proc., Thirteenth Annual Asilomar Conference on Circuits, Systems, and Computers, Pacific Grove, California, November 5-7, 1979.

[McCluskey, 1979b] McCluskey, E.J., "Fault Tolerant Computing Systems," Tech. Note No. 170, Computer Systems Laboratory, Stanford University, Stanford, California, November 1979.

[McCluskey, 1979c] McCluskey, E.J., "Testing and Diagnosis of Logic," Proc., Euro/IFIP 79, P.A. Samet, Editor, London, England, September 25-28, 1979; North-Holland Publishing Company, Oxford, England, 1979.

[Miller, 1979] Miller, D.H., "A Taxomony of Fault-Tolerant Techniques," Tech. Note No. 175, Computer Systems Laboratory, Stanford University, Stanford, California, June 1979.

[Pradhan, 1980] Pradhan, D.K., "Design of Easily Testable Sequential Machines Using Extra Inputs," Tech. Note No. 173, Computer Systems Laboratory, Stanford University, Stanford, California, January 1980.

4 MEETINGS

In addition to publishing scientific articles, CRC personnel participated in the following technical conferences and meetings:

1. Ninth Annual Fault-Tolerant Computing Symposium (FTCS-9), Madison, Wisconsin, June 20-22, 1979, attended by E.J. McCluskey and Behzad Khodadad.

2. AIAA Computers in Aerospace Conference II, Los Angeles, California, October 22-24, 1979, attended by E.J. McCluskey.

3. Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, California, November 5-7, 1979, attended by E.J. McCluskey.

4. COMPCON Spring 80, San Francisco, California, February 25-28, 1980, attended by E.J. McCluskey.

5. Workshop on Fault Tolerant VLSI Design, Santa Monica, California, April 23-25, 1980, attended by E.J. McCluskey.

6. IEEE Workshop on Design for Testability, Boulder, Colorado, April 16-17, 1980, attended by E.J. McCluskey.

7. Computer Elements Committee Workshop, Vail, Colorado, June 22-25, 1980, attended by E.J. McCluskey.

8. 10th Annual Fault-Tolerant Computing Symposium, Kyoto, Japan, October 1-3, 1980, attended by E.J. McCluskey, P.L. Fu, R.K. Iyer and D.J. Lu.

5 PERSONNEL

Principal Investigator:	E. J. McCluskey, Professor Depts. of Electrical Engineering and Computer Science
Research Staff:	M. Danielle Beaudry, Research Associate Dept. of Electrical Engineering May 1979 to June 1979
	Ravishankar K. Iyer, Research Associate Dept. of Electrical Engineering October 1980-; Visitor from CSIRO Canberra, Australia August 1979 - September 1980
Visiting Professor:	Dhiraj K. Pradhan School of Engineering Oakland University Rochester, Michigan
Research Assistants:	Steve Butner, Electrical Engineering Peter L. Fu, Electrical Engineering Behzad khodadad, Electrical Engineering Daniel Miller, Electrical Engineering Jacob Savir, Electrical Engineering

6 RESUMES

E. J. McCLUSKEY

BIOGRAPHY

ADDRESS: Center for Reliable Computing, Computer Systems Laboratory, Stanford University, Stanford Ca. 94305 (415) 497-1451

BORN: October 16,1929, New York,N.Y.

EDUCATION: Sc.D. (E.E.) M.I.T., 1956; B.S. and M.S. (E.E.) M.I.T., 1953
A.B. (Physics, Math.), Summa Cum Laude, Bowdoin College, 1953

POSITIONS:
Stanford University
Professor of Electrical Engineering and Computer Science, 1967-
Director, Digital Systems Laboratory, 1969-1978
Director, Stanford Computer Forum, 1969-1978
Chairman, Computer Engineering Program, 1970-1981
Princeton University
Professor of Electrical Engineering, 1963-1966
Director of Computer Center, 1961-1966
Associate Professor of Electrical Engineering, 1959-1963
Bell Telephone Laboratories
Technical Staff, Electronic Telephone Office Design, 1955-1959

CONSULTING: Digital Equipment Corporation, 1980; Xerox Corporation, 1979; Battelle, 1978; Hughes Aircraft Corporation, 1978; Honeywell Corporation, 1977; Microtechnology Corporation, 1977; Payln Associates, Inc., 1973-1975; Signetics Corporation, 1971-1980; IBM Scientific Center (Palo Alto, California), 1966-1967; Scientific Advisory Groups, General Precision, 1962-1966; IDA Task Force on Computers in Command and Control, 1962

SUMMER POSITIONS: IBM Watson Research Center Distinguished Visiting Faculty, 1979; JSPS Fellowship, Tokyo and Kyoto Universities, 1978; RCA, Design Automation, 1966; MIT Lincoln Laboratory, Computers in C~f~Command and Control,1961; IBM, NOR Gate Design, 1960

PROFESSIONAL SOCIETY POSITIONS AND HONORS:
AAAS Fellow, 1967
ACM National Lectureship, 1965-1966; Curriculum Committee, 1967-1969; SIGARCH Director, 1980
AFIPS Executive Committee, 1972-1974; Director, 1970-1974
IEEE Fellow Committee, 1979-80; Long Range Planning Committee, 1971; Proceedings Editorial Board, 1966-1968; Fellow, 1965
IEEE COMPUTER GROUP Chairman, 1970; San Francisco Computer Chapter Chairman, 1969-1970
IEEE COMPUTER SOCIETY President, 1970-1971

CONFERENCE ACTIVITIES (selected):

USA Program Chairman, 3rd USA-Japan Computer Conference, San Francisco, California, October 10-12, 1978

General Chairman, 5th Annual Symposium on Computer Architecture, Palo Alto, California, April 3-5, 1978

General Conference Chairman, 1973 International Symposium on Fault-Tolerant Computing (FTCS-3), June 1973

General Chairman, Third Symposium on Operating Systems, 1971

SEMINARS AND INVITED LECTURES AND PAPERS (selected):

"Testing and Diagnosis of Logic," Invited Paper, Euro/IFIP 79, P.A. Samet, Editor, London, England, September 25-28, 1979

"Logic Design for Multi-Level Integrated Circuits," Distinguished Lecturer Series, Computer Science Dept., Carnegie-Mellon University, Pittsburgh, Pennsylvania, March 8, 1978

OTHER PROFESSIONAL ACTIVITIES:

The Annals of the History of Computing, Editorial Board, AFIPS, 1978-

Design Automation and Fault-Tolerant Computing, Editorial Board, 1977-

Digital Processes, Editorial Board, Delta Publishing Company, Ltd., Switzerland, 1975-

Computer Design and Architecture Series, Elsevier North-Holland, Inc. (formerly American Elsevier), New York, 1973-

Visiting Committee for Information and Computer Science, Georgia Institute for Technology, 1978

Patentee with T.T. Dao and L.K. Russell, "Multivalued Integrated Injection Logic Circuitry and Method," No.4,140,920, February 20, 1979

National Academy of Science, Planning Group for Education, Computer Science and Engineering Board, 1968-1973

Commission on Engineering Education COSINE Committee, 1965-1972

SELECTED PUBLICATIONS

Books

INTRODUCTION to the THEORY of SWITCHING CIRCUITS, McGraw-Hill Book Co., New York, New York, 1965.

DESIGN of DIGITAL COMPUTERS, with H.W., Gschwind, Springer-Verlag, New York, New York, 1975.

"Logic Design," ENCYCLOPEDIA OF COMPUTER SCIENCE, 2ND EDITION, A.Ralston, Editor, Petrocelli/Charter, New York, New York, 1980.

Journal Papers

"Minimization of Boolean Functions," B.S.T.J., Vol. 35, No. 6, pp. 1417-1444, November 1956.

"Iterative Combinational Switching Networks - General Design Considerations," IRE Trans. on Electronic Computers, Vol. EC-7, No. 4, pp. 285-291, December 1958.

"Error-Correcting Codes - A Linear Programming Approach," B.S.T.J., Vol. 38, No. 6, pp. 1485-1512, November 1959.

(With S.H. Unger) "A Note on the Number of Internal Variable Assignments for Sequential Switching Circuits," IRE Trans. on Electronic Computers, Vol. EC-8, No. 4, pp. 439-440, December 1959.

(With M.C. Paul) "Boolean Functions Realizable with Single Threshold Devices," Proc., IRE, Vol. 48, No. 7, pp. 1335-1337, July 1960.

(With F.W. Clegg) "Fault Equivalence in Combinational Logic Networks, IEEE Trans. on Computers, Vol. C-20, No. 11, pp. 1286-1293, November 1971.

(With D.P. Siewiorek) "An Iterative Cell Switch Design for Hybrid Redundancy ," IEEE Trans. on Computers, Vol C-22, No. 3, pp. 290-297, March 1973.

(With K.P. Parker) "Analysis of Logic Circuits with Faults Using Input Signal Probabilities," IEEE Trans. on Computers, Vol. C-24, No. 5, pp. 573-578, May 1975.

(With J.J. Shedletsky) "The Error Latency of a Fault in a Sequential Digital Circuit," IEEE Trans. on Computers, Vol. C-25, No. 6, pp. 665-659, June 1976.

"Logic Design of Multi-Valued IIL Logic Circuits," IEEE Trans. on Computers, Vol. C-28, No. 8, pp. 546-559, August 1979.

(With J.P. Hayes) "Testability Considerations in Microprocessor-Based Design," Computer Magazine, pp.17-26, March 1980.

Conference Papers

(With A. Grasselli) "Une Version Modifiee D'Algol Pour La Programmation Logique (1)," Proc., 2 eme Congress de l'Association Francaise de Calcul et de Traitement de l'Information, Paris, France, October 7-20, 1961.

"Transients in Combinational Logic Circuits," REDUNDANCY TECHNIQUES for COMPUTING SYSTEMS, pp. 9-46, R.H. Wilcox and W.C. Mann, Editors, Spartan Books, Washington, D.C., 1962.

"Fundamental Mode and Pulse Mode Sequential Circuits," Proc., 2nd Int'l Federation on Information Processing Congress, pp. 725-730, Munich, West Germany, August 27- September 1, 1962 (North-Holland Publishing Company, Amsterdam, Netherlands).

"Logical Design Theory of NOR Gate Networks with No Complemented Inputs," Proc., 4th Annual Symposium on Switching Circuit Theory and Logical Design, S-156, pp. 137-148, IEEE, Chicago, Illinois, September 1963.

(With J.F. Wakerly) "Design of Low-Cost General-Purpose Self-Diagnosing Computers," Proc., IFIP Congress '74, pp. 108-111, Stockholm, Sweden, August 3-10, 1974.

(With T.T. Dao, L.K. Russell and D.R. Preedy) "Multilevel IIL with Threshold Gates," Proc., IEEE Int'l Solid-State Circuits Conference, Philadelphia, Pennsylvania, February 16-18, 1977.

(With J.F. Wakerly) "Microcomputers in the Computer Engineering Curriculum," Microprocessors-2, Invited Papers, Infotech Int'l Ltd., Berkshire, England, 1977.

(With S. Bozorgui-Nesbat) "Design for Autonomous Test," PROC. 1980 TEST CONFERENCE, Philadelphia, Pennsylvania, November

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(With W.F. Atchison, S.D. Conte, J.W. Hamblen, T.E. Hull, T.A. Keenan, W.B. Kehl, S.O. Navarro, W.C. Rheinboldt, E.J. Schweppe, W. J. Viavant, and D.M. Young) "Curriculum 68," Communications of the ACM Vol. II, No. 3, pp. 151-197, March 1968.

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BIOGRAPHY

BORN: Washington, D.C., 18 October 1947

EDUCATION:

B.S.	M.I.T.	Physics	1969
M.S.	Stanford	Electrical Engineering	1974
M.S.	Stanford	Statistics	1977
Ph.D.	Stanford	Electrical Engineering with Computer Science minor	1978

EDUCATIONAL HONORS:

National Merit Scholarship 1965-1969
National Honor Society Scholarship (declined) 1965
IBM Graduate Fellowship 1974-1976

PROFESSIONAL ACTIVITIES:

Member of AAAS, ACM, IEEE Computer Society, SWE, WISE, Sigma Xi
Treasurer of Santa Clara Group of IEEE Computer Society (1977-1978)
Publicity Chairwoman for Fifth Annual Symposium on Computer Architecture, Palo Alto, 3-5 April 1978
Session Chairwoman for 3rd USA-Japan Computer Conference, San Francisco, 10-12 October 1978

PROFESSIONAL EXPERIENCE:

Lecturer in Computer Science (April-June 1979)

Computer Science Department, Stanford University

Computer Science 105, Introduction to Computing. Undergraduate course using the programming language PASCAL.

Research Associate (April 1978 - present)

Center for Reliable Computing, Computer Systems Laboratory
Stanford University

Research on performance and reliability evaluation of computing systems. Supervisor: Prof. Edward J. McCluskey.

Teaching assistant (October-December 1977)

Electrical Engineering Department, Stanford University

Computer Science 311, (also Electrical Engineering 482), Advanced Computer Organization. Graduate course in computer architeture.

Research assistant (July 1976 - September 1977 and January-April 1978)

Digital Systems Laboratory, Stanford University

Research on the performance and reliability of gracefully degrading computing systems. Supervisor: Prof. Edward J. McCluskey.

IBM Graduate fellow (October 1974 - June 1976)

Digital Systems Laboratory, Stanford University

Research on dual redundant and gracefully degrading computer systems. Supervisor: Prof. Edward J. McCluskey.

Research assistant (April 1974 - September 1974)

Digital Systems Laboratory, Stanford University

Research on dual redundant computer systems.
Supervisor: Prof. Edward J. McCluskey.

Systems engineer (April 1973 - March 1974)

Hewlett-Packard Corporation, Santa Clara, California

Programming support for graphics package and instrument interfaces for Fourier Analyzer computer systems.

Programmer (October 1969 - March 1973)

Fairchild Semiconductor, Mountain View, California

Programming in computer-aided design of integrated circuits.

CONSULTING:

National Semiconductor, 1978
Hughes, 1978-
Technology Development Corporation, 1979

PUBLICATIONS:

"A Markov model for reconfigurable computer systems," (with E. Fregni), Tech. Note No. 43, Digital Systems Lab., Stanford Univ., 1974.

"Dual redundancy -- a survey," Tech. Note No. 93, Digital Systems Lab., Stanford Univ., April 1977.

"Performance related reliability measures for computing systems," Tech. Note No. 101, Digital Systems Lab., 1976.

"Performance-related reliability measures for computing systems," Proc. FTCS-7, 7th Annual International Conference on Fault-Tolerant Computing, pp. 16-21, June 1977.

"Performance considerations for the reliability analysis of computing systems," Ph.D. Dissertation, Stanford Univ., April 1978.

"Performance considerations for reliability analysis: A statistical case study," Tech. Note. No. 126, Digital Systems Lab., Stanford Univ., 1978.

"A statistical analysis of service interruptions at the SLAC Triplex multiprocessor," Tech. Rpt. No. 141, Digital Systems Lab., 1978.

"Performance considerations for reliability analysis: A statistical case study," Proc. FTCS-8, Eighth Annual International Conference on Fault-Tolerant Computing, Toulouse, France, p. 198, June 1978.

"Performance-related reliability measures for computing systems," IEEE Trans. on Computers, Special Issue on Fault-Tolerant Computing, June 1978, pp. 540-547.

"A statistical analysis of failures in the SLAC computing center," Digest of Papers, Spring COMPCON 79, San Francisco, CA, pp. 49-52, 26 February - 1 March 1979.

"Stochastic behavior of failures in computing systems," Tech. Note, Computer Systems Lab., (in preparation).

Curriculum Vitae

1.	FULL NAME	RAVISHANKAR KRISHNAN IYER
2.	ADDRESS	CENTER FOR RELIABLE COMPUTING COMPUTER SYSTEMS LABORATORY Departments of Electrical Engineering and Computer Science Stanford University Stanford CA 94305 Ph. 415-497-1448; 415-323-9112.
3.	DATE AND PLACE OF BIRTH	4 December 1949, New Delhi India.
4.	NATIONALITY	Australian
5.	MARITAL STATUS	Single
6.	DETAILS OF EDUCATION CAREER	(i) B.E. (Electrical) Electronics Communication, 1973. University of Queensland Brisbane, Australia. (ii) M.Eng.Sc(Qual.) 1974. (iii) Ph.D 1977, University of Queensland, Australia.
7.	PRIZES AND AWARDS	(i) Prize and plaque for a research paper (graduate category) IEEE Student paper contest 1977. (ii) Best Australian student paper, IEEE (Australian section) prize, 1977. (iii) Royal Norwegian Council for Scientific and Industrial Research Fellowship 1977. (iv) CSIRO (Commonwealth Scientific and Industrial Research Organization, Australia) Postdoctoral scholarship (for young scientists) 1978. (v) IBM World Trade Visiting Scientist, T. J. Watson Center, 1980.

8. ACADEMIC AND PROFESSIONAL EXPERIENCE

(a) Tutor in Electrical Engineering
University of Queensland 1973-1977.

(b) Norwegian Institute of Technology
University of Trondhiem, Norway 1977-1979.

(c) Computer Systems Laboratory
Stanford University 1979 -
(on CSIRO Fellowship).

(d) Visiting Lectures and Seminars
University of Stuttgart, W. Germany.
Danish Technical University, Denmark
University of Lund, L. M. Ericsson, Sweden.

(e) Referee, reliability journals
and conferences.

9. PROFESIONAL AFILIATION Member IEEE

10. RESEARCH WORK

During the past 6 years or so I have been engaged in developing probabilistic models for studying system performance degradation. Particular attention has been paid to modelling computer systems; two major classes of problems have been studied:

A) Reliability Analysis and Design (catastrophic failure, fault tolerance, transient errors).

B) Performance Evaluation (including overflow streams, feedback and priority queues).

In Australia sections of this work were supported by Telecom Australia, The Radio Research Board, The Electrical Research Board and The Queensland Electrical Authorities Research Committee.

In Norway the research was supported by The Norwegian Telecommunications Administration Research Establishment.

Brief descriptions of the problems investigated in each of the above areas appears below:

A. (1) Reliability Modelling, Fault Tolerance.

a) Optimal reliability design of series-parallel systems [2].

b) Evaluation and optimization of the reliability of complex structures [4] [5].

c) Fault tolerant configurations [15].

d) Study of the effect of uncertainty in failure rate prediction on the reliability and performance of fault tolerant sytems [18].

(2) Transient Error Analysis

a) An analytical model for the transient error generation process [14].

b) Optimal allocation of check-points and rollback intervals [14].

(3) Prediction of Software Reliability

a) Development of a finite sampling model.

b) A Bayesian approach to failure rate estimation.

B. (1) Performance Studies.

a) Statistical analysis of system load and failures at the Stanford Linear accelerator Computer multiprocessor) [18].

b) Analysis of system behaviour due to variations in system component qualities (grades or tolerances) [1], [6].

c) Intermittent failures; effect on performance: Development of a shock model.

(2) Approximate Techniques for the Analysis of Feedback and Priority Queues in Computer Systems.

A job/task graph formulation has been proposed to describe te workload on a system. Three approaches to generating approximating solutions are being studied and their goodness tested by simulation [16].

a) Piece-wise models

b) A modified Taylor approximation model.

c) A state dependent level crossing formulation.

(3) Study of Overflow Streams [10].

(4) A Multiserver Model for a Metropolitan Telephone Network [8].

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ITEM #20, CONTINUED: author summarizes the important results in each of the above problem areas.


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